Monday, November 24, 2008

Poster Session

9:00~10:00/12:35~13:45 2nd Floor Lobby

**Analog and Mixed-Signal Circuits**

**Session Chair** Donghyun Bak (Chung-Ang University, Korea)

**Co Chair** Kyoungrok Cho (Chungbuk National University, Korea)

**P-1** A New Design Method to Reduce the Power Consumption in a Flash-A/D Converter
Soon-Ik Cho, Soon-Kyung Choi, Suki Kim (Korea University, Korea), Kwang-Hyun Baek (Chung-Ang University, Korea)

**P-2** Spread Spectrum Clock Generator for DisplayPort
Hyun-Chul Lee, Suk-Won Lee, Jin-Ku Kang (Inha University, Korea)

**P-3** A Design Guide for 3-stage CMOS Nested Gm-C Operational Amplifier with Area or Current Minimization
Jae-Seung Lee, Jae-Yoon Sim, Hong June Park (POSTECH, Korea)

**P-4** A 2.7Gbps & 1.62Gbps Dual-Mode Clock and Data Recovery for DisplayPort
Seungwon Lee, Jae-Wook Yoo, Jin-Ku Kang (Inha University, Korea)

**P-5** A CMOS Linear Preamplifier Design for Electret Microphones
Gil-Seop Park, Seung-Tak Ryu (Information and Communications University, Korea)

**Communication SoCs**

**P-6** A study of Detection algorithm for DAA regulation of Korea using MB-OFDM UWB Receiver
Cheol-Ho Shin, ByoungHak Kim, Sangsung Choi (ETRI, Korea)

**P-7** Implementation of FlexRay Protocol with An Automotive Application
Yi-Nan Xu, I. G. Jang, Y. E. Kim, J. G. Chung (Chonbuk National University, Korea), Sung-Chul Lee (KETI, Korea)

**P-8** New Sum-Product Algorithm Using Approximation Method for Low Complexity LDPC Decoding
Jae Hee Han, Myung Hoon Sunwoo (Ajou University, Korea)

**P-9** Efficient CTC Interleaver and Deinterleaver for the WiMAX Standard
Kon-Woo Kwon, Jeongwoo Park, Bongchoon Lee, Suki Kim (Korea University, Korea), Kwang-Hyun Baek (Chung-Ang University, Korea)

**P-10** Low Complexity Soft-Decision Demapper for High Order Modulation of DVB-S2 system
Jang Woong Park, Myung Hoon Sunwoo (Ajou University, Korea), Pan Soo Kim, Dae-Ig Chang (ETRI, Korea)

**P-11** Implementation of DCT based OFDM system
Gi Hyun Kim, Honey Durga Tiwari, Chan Mo Kim, Yong Beom Cho, Younggoo Kwon (Konkuk University, Korea)

**Display Driver and Imaging Devices and interfaces**

**P-12** A Design of DisplayPort Link Layer
Yong-woo Kim, Seong-bok Cha, Jin-ku Kang (Inha University, Korea)
**P-13** A 5-Gb/s Continuous-time Adaptive Equalizer and CDR using 0.18 $\mu$m CMOS
Tae-Ho Kim, Sang-Ho Kim, Jin-Ku Kang (Inha University, Korea)

**P-14** Software Implementation of TPEG Decoder for T-DMB using X-PAD
Kyo-Seok Kim, Soon-Tae Kwon, Jun-dong Cho (SungKyungKwan University, Korea), Min-Kyu Kim, Je-hyuk Ryu, Kyung-Uk Kim (Samsung Electro-Mechanics, Korea)

**P-15** Design of Application Specific Processor for H.264 Inverse Transform and Quantization
Jae-Jin Lee, SeongMo Park, NakWoong Eum (ETRI, Korea)

**P-16** Design and implementation of 16-bit fixed point digital signal processor
Donghoon Lee, Changwon Ryu, Jusung Park (Pusan National University, Korea), Kyunsoo Kwon, Wontae Choi (Samsung Electro-Mechanics, Korea)

**P-17** Multiplier design based on ancient Indian Vedic Mathematics
Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho (Konkuk University, Korea)

**Low Power Design Techniques**

**P-18** Design of High Energy Efficiency 32bit Processing Unit using Instruction- Levels Data Gating and Dynamic Voltage Scaling Techniques
Yil Suk Yang, Tae Moon Roh, Soon il Yeo (ETRI, Korea), Woo H. Kwon (Kyungpook National University, Korea), Jongdae Kim (ETRI, Korea)

**P-19** A New Scheduling Technique Based on Dynamic Voltage Scaling for MPSoC
Chang-Woo Park, Kyung-Woo Noh, Seok-Yoon Kim (Soongsil University, Korea)

**P-20** Low-power Dynamic Scheduling Algorithm For Real-time Multiprocessor Systems
Se-Jin Ko, Ki-Young Kim, Seok-Yoon Kim (Soongsil University, Korea)

**P-21** A Novel Dynamic Power Management Technique for Multi-Core based Mobile Devices
Youngho Ahn, Young-Si Hwang, Ki-Seok Chung (Hanyang University, Korea)

**P-22** Selective Multiplexer-Removal Algorithm for Lowering Power Consumption of Circuits
Chi-Hoon Shin (University of Science and Technology, Korea), Myeong-Hoon Oh, Young-Woo Kim, Sung-Nam Kim, Seong-Woon Kim (ETRI, Korea)

**P-23** Digital Power Estimation Flow Combining Academic and Industrial Tools
R. Mehrotra, T. English, K.L. Man, E. Popovici, M.P. Schellekens (University College Cork, Ireland)

**Multimedia (A/V) SoCs**

**P-24** Enhanced Parallel Decoding for H.264/AVC CAVLC by Using Precomputation
Donghoon Yeo, Hyunchul Shin (Hanyang University, Korea)

**P-25** Implementation of 3D Graphics Accelerator using Full Pipeline Scheme on FPGA
Kyungsu Kim, Hoosung-Lee, Seonhyun Cho, Seongmo Park (ETRI, Korea)
**P-26** Hardware Implementation of Motion Estimation Using a Sub-sampled Block for Frame Rate Up-Conversion  
Suk-Ju Kang, Dong-Gon Yoo, Sung-Kyu Lee, Young Hwan Kim (POSTECH, Korea)

**P-27** Design of Voice Guiding System Using Serial Connection Technique of Speakers  
Jisung Byun, Sunyong Lee, Teawan Kim, Jungsu Park, Yunmo Chung (Kyung Hee University, Korea), Moonvin Song, Ohkyun Kwon (Marincom Co., Korea sprite Co., Korea)

**P-28** Design of a Motion Compensation Unit for H.264 Decoder using 2-Dimensional Circular Register Files  
Chanho Lee, Yonghoon Yu (Soongsil University, Korea)

**P-29** A Synchronous DRAM Controller for an H.264/AVC Encoder  
Gyounghwan Hyun, Yongseok Jin, Jinsu Jung, Seongyoon Kim, Hyuk-Jae Lee (Seoul National University, Korea)

**P-30** Simplified NAL Decoder for H.264/AVC Baseline Profile  
Kwangrae Jeong, Jinha Choi, Jaeseok Kim (Yonsei University, Korea)

**P-31** Image Quality Enhancement by Real-Time Gamma Correction for a CMOS Image Sensor in Mobile Phones  
Hyowon Jeong (Dong-A University, Korea), Joohyun Kim, Wontae Choi (Samsung Electro-Mechanics, Korea), Bongsoon Kang (Dong-A University, Korea)

**P-32** An Efficient color Demosaicing Using Approximated Directional Line Averages  
Yang-Ki Cho, Joo-Seok lee (Embedded System R&D Center, Korea), Hyeon-mi Yang, Hi-Seok Kim (Cheongju University, Korea)

**P-33** A Unified Transform Unit for H.264  
Sehyun Song, Changwoo Seo, Kichul Kim (University of Seoul, Korea)

**P-34** The Compensation system for the event in the fuel cell mobile phone  
Chung-Ho Shin, Jun-Dong Cho (Sungkyunkwan University, Korea)

**RF ICs and Signal integrity**

**P-35** Wideband LPF for WiMedia UWB RF transceiver  
Seung-Sik Lee, Seong-Hyun Jang, Bong-Hyuk Park, Sang-Sung Choi (ETRI, Korea)

**P-36** A 1.2V 3 ~ 8 GHz Low Noise Amplifier in 0.13 μm CMOS  
Bonghyuk Park, Seung Sik Lee, Seunghyun Jang, Sangsung Choi (ETRI, Korea)

**P-37** RF Receiver Chip Set Employing 0.13 μm CMOS Technology for Application to K-band Commercial Automotive Radar System  
Young-Bae Park, Se-Ho Kim, Young Yun (Korea Maritime University, Korea), Kyu-Ho Park, Kwang-Ho Ahn, Kim Ki-Jin, Kim Jin-Sup, Choi Se-Hwan (KETI, Korea)

**P-38** A linear wideband CMOS LNA for 3-5 GHz UWB systems  
Ali Mirvakili (K.N. Toosi University of Technology, Iran), Mohammad Yavari (Amirkabir University, Iran)

**P-39** Discontinuous RC Interconnect Line Analysis for Accurate Timing Determination  
Taehoon Kim, Youngdoo Song, Yungseon Eo (Hanyang University, Korea)
P-40 CROSSTALK AVOIDANCE METHOD CONSIDERING MULTI-AGGRESSORS
Sibaek Jung (Hynix semiconductor Inc., Korea), Naeun Zang, Eunsuk Park, Juho Kim (Sogang University, Korea)

P-41 PERFORMANCE ANALYSIS OF NOC STRUCTURE BASED ON STAR-MESH TOPOLOGY
Juyeob Kim, Miyoung Lee, Wonjong Kim, Junyoung Chang, Younghwan Bae, Hanjin Cho (ETRI, Korea)

P-42 POWER SUPPLY NOISE REDUCTION BY CLOCK SCHEDULING WITH GATE-LEVEL CURRENT WAVEFORM ESTIMATION
Yooseong Kim, Sangwook Han, Juho Kim (Sogang University, Korea)

P-43 STAR-MESH NOC BASED MULTI-CHANNEL H.264 DECODER DESIGN
June-Young Chang, Won-Jong Kim, Young-Hwan Bae, Mi-Young Lee, Ju-Yeob Kim, Han-Jin Cho (ETRI, Korea)

P-44 THE USE OF FAIR Y-SIM FOR OPTIMIZING MAPPING SET SELECTION IN HARDWARE/SOFTWARE CO-DESIGN
Olufemi Adeluyi, Eun-ok Kim, Jeong-A Lee (Chosun University, Korea), Jeong-Gun Lee (Hallym University, Korea)

P-45 A DESIGN VERIFICATION KIT FOR PASSIVE RFID SYSTEM ON A CHIP
Chan-Won Park (ETRI, Korea), Bo-Gwan Kim (Chungnam National University, Korea)

P-46 LEVERAGING CMOS DESIGN TOOLS FOR QCA DESIGNS
Kyosun Kim, Younbo Oh (University of Incheon, Korea), Ramesh Karri (Polytechnic University, USA), Alex Orailoglu (University of California, USA)

P-47 ASSESSMENT OF USING THE STATISTICAL TIMING ANALYSIS SOFTWARE FOR THE VLSI DESIGN AT THE MACRO LEVEL
Hyung Gyun Yang, Wook Kim, Young Hwan Kim (POSTECH, Korea)

P-48 OPERATION ABOUT MULTIPLE SCAN CHAINS BASED ON SYSTEM-ON-CHIP
Insoo Kim, Hyoung Bok Min (Sungkyunkwan University, Korea)

P-49 A PROGRAMMABLE MEMORY BIST FOR EMBEDDED MEMORY
WonGi Hong, JungDai Choi, Hoon Chang (Soongsil University, Korea)

P-50 PATH DELAY FAULT DIAGNOSIS USING PATH SCORING
Yoseop Lim, Joohwan Lee, Sungho Kang (Yonsei University, Korea)
Chip Design Contest - Exhibition Session

9:00~10:00/12:35~13:45  2nd Floor Lobby

**CDC-3**  Automatic Red-eye Detection and Correction System for Mobile Devices
Wonwoo Jang, Chris sungjin Lee (Dong-A University, Korea), Sukchan Kim (Pusan National University, Korea), Bongsoon Kang (Dong-A University, Korea)

**CDC-4**  Design of Rasterization unit Applicable to Mobile Graphics System
Seung-Hyun Lee, Chang-Soo Ha, Sung-Jin Lee, Byeong-Yoon Choi (Dongeui University, Korea)

**CDC-6**  Design of On-Chip Debug System for embedded processor
Hyungbae Park, Jingzhe Xu, Jusung Park, Jung-Hoon Ji, Gyun Woo (Pusan National University, Korea)

**CDC-7**  Design & Verification of 16 Bit RISC Processor
Seung Pyo Jung, Jingzhe Xu, Donghoo Lee, Ju Sung Park (Pusan National University, Korea), Kang-joo Kim, Koon-shik Cho (Samsung Electro-Mechanics, Korea)

**CDC-9**  A 8 Gb/s 4-PAM Transmitter in 0.18 μm CMOS Technology
Hyunkyo Kim, Jungjoon Lee, Jikyung Jung, Jinwook Burm (Sogang University, Korea)

**CDC-11**  High performance IPC hardware accelerator and communication network for MPSoCs
Moonmo Koo, Soo-Ik Chae (Seoul National University, Korea)

**CDC-13**  ODALRISC: A Small, Low Power, and Configurable 32-bit RISC Processor
Imyong Lee, Dongwook Lee, Kiyoungh Choi (Seoul National University, Korea)

**CDC-15**  Chip Implementation of a Coarse-Grained Reconfigurable Architecture Supporting Floating-Point Operations
Manhwee Jo, Dongwook Lee, Kiyoungh Choi (Seoul National University, Korea)

**CDC-17**  High Performance On-Chip-Network Architecture with Multiple Channels and Dual Routing
Byungyong Kim, Chanho Lee (Soongsil University, Korea)

**CDC-20**  Design of Memory Controller -Design of General purpose Memory Controller
Park soo il, Song jae yeol, Park seok hwi, Jung jihoon (Chonnam University, Korea)

**CDC-23**  Design of Parallel BCH Decoder for MLC Memory
Song-Chul Jang, Je-Hoon Lee, Won-Chul Lee, Kyoung-Rok Cho (Chungbuk National University, Korea)

**CDC-24**  SoC Platform Design with Multi-Channel Bus Architecture
Younjin Jung, Ok Kim, Byoungyup Lee, Hongkyun Jung, Kwangki Ryoo (Hanbat National University, Korea)

**CDC-27**  Design of High-Performance 32-bit Embedded Processor
Ji-Hoon Kim, Duk-Hyun You (KAIST, Korea), Ki-Seok Kwon (Samsung Advanced Institute of Technology, Korea), Eun-Joo Bae, WonHee Son, In-Cheol Park (KAIST, Korea)
**CDC-28** Design of a Scalable Sound Synthesizer  
Tae-Hwan Kim, Young-Joo Lee, In-Cheol Park  
(KAIST, Korea)

**CDC-30** Implementation of Efficient Architecture of  
Two-Dimensional Discrete Wavelet Transform  
Jinook Song, In-Cheol Park (KAIST, Korea)

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**Chip Design Contest - Poster Session**

<table>
<thead>
<tr>
<th>Time</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:00~9:30(Presentation)</td>
<td>Room 202</td>
</tr>
<tr>
<td>9:00<del>10:00/12:35</del>13:45</td>
<td>2nd Floor Lobby</td>
</tr>
</tbody>
</table>

**CDC-1** 12-bit 80MSPS Double Folding/Interpolation  
A/D Converter  
Byungil Kim, Daeyun Kim, Jooho Hwang, Junho Moon, Minkyu Song (Dongguk University, Korea)

**CDC-2** 10-bit Charge Redistributed D/A Converter  
for TFT-LCD Driver  
Juneseok Lee, Doobock Lee, Hyosang Kim, Junho Moon, Minkyu Song (Dongguk University, Korea)

**CDC-5** Design of 24 bit DSP for audio algorithms  
Chang Won Ryu, Seung Jae Hwang, Ju Sung Park  
(Pusan National University, Korea)

**CDC-8** Implementation of the Levinson Algorithm  
for MMSE Equalizer  
Minsu Kim, Jinyong Lee, Younglok Kim (Sogang University, Korea)

**CDC-10** Efficient Implementation of Linear System  
Solution Block using LDLT Factorization  
Hanjoon Cho, Jinyong Lee, Younglok Kim (Sogang University, Korea)

**CDC-12** Multi-Channel Capacitive Readout IC for  
MEMS Inertial Sensors  
Wook Bahn, Hyoungho Ko, Cheol-kyu Han, Sangyoon Lee, Deog-kyoon Jeong, Dong-il ‘Dan’ Cho (Seoul National University, Korea), Taedong Ahn, Kwangho Yoo (SML Electronic, Inc., Korea)

**CDC-14** A Concurrent Dual-Band CMOS Low-Noise  
Amplifier for ISM-Band Application  
Hee Sauk Jhon, Hakchul Jung, MinSuk Koo, Hyungcheol Shin (Seoul National University, Korea)

**CDC-16** High Speed 3D Acquisition Chip Design  
for Robot Applications  
Byung-Joo Hong, Seung-Hoon Lee, Jun-Dong Cho  
(Sungkyunkwan University, Korea), Je-Hyuk Ryu  
(Samsung Electro-Mechanics, Korea)

**CDC-18** A/D Converter using Iterative Divide-by-Two Reference for CMOS Image Sensor  
Jeonghwan Lee, Gunhee Han (Yonsei University, Korea)

**CDC-19** Design of a Flash A/D Converter with  
Dual-bootstrapped THA circuit  
Young-jun Son, Won Kim, Kwang-sub Yoon (Inha University, Korea)

**CDC-21** Varactor Tuned High-Q Active Inductor  
with Broadband Tuning Range  
Kyungji Song, Heungjae Choi, Yongchae Jeong  
(Chonbuk National University, Korea)

**CDC-22** Design of Low-Power and High-Speed  
Receiver for Mobile Display Module  
Cheon-Hyo Lee, Jeong-Hoon Kim, Jae-Hyung Lee, Liyan Jin, Yong-Hu Yin, Ji-Hye Jang, Min-Cheol Kang, Pan-Bong Ha, Young-Hee Kim (Changwon National University, Korea)
**Conference Information**

**Registration Fees**

<table>
<thead>
<tr>
<th>Category</th>
<th>Regular</th>
<th>Student</th>
</tr>
</thead>
<tbody>
<tr>
<td>Early Registration By October 15, 2008</td>
<td>$ 200</td>
<td>$ 70</td>
</tr>
<tr>
<td></td>
<td>(200,000KRW)</td>
<td>(70,000KRW)</td>
</tr>
<tr>
<td>Non-Members</td>
<td>$ 220</td>
<td>$ 100</td>
</tr>
<tr>
<td></td>
<td>(220,000KRW)</td>
<td>(100,000KRW)</td>
</tr>
<tr>
<td>Registration After October 15, 2008</td>
<td>$ 220</td>
<td>$ 100</td>
</tr>
<tr>
<td></td>
<td>(220,000KRW)</td>
<td>(100,000KRW)</td>
</tr>
<tr>
<td>Non-Members</td>
<td>$ 250</td>
<td>$ 120</td>
</tr>
<tr>
<td></td>
<td>(250,000KRW)</td>
<td>(120,000KRW)</td>
</tr>
</tbody>
</table>

※ Regular/Student Registration Entitlements
- Admission to all sessions
- CD-ROM, Final program
- Coffee break
- Banquet (Student participants are also eligible for free banquet)
- You must make an early-registration or online-registration to be eligible for free banquet.
- After the online registration due date, including on the conference day, you have to purchase a banquet ticket if you want to enjoy a banquet. Ticket availability will depend on the available banquet spaces.

**Emergency Calls**

Professor Joong-Ho Choi (Conf. Secretary)
Mobile : 010-2749-2510

Professor Chang-Wan Kim (Local arrangement)
Mobile : 016-533-2737
**Special Programs**

**Best Paper Awards**

**Regular Oral Session**
- ISOCC Best Paper
- IEEK (The Institute of Electronics Engineers of Korea) Best Paper
- Semiconductor & Device Society of IEEK (The Institute of Electronics Engineers of Korea) Best Paper
- SoC Design Group of IEEK (The Institute of Electronics Engineers of Korea) Best Paper
- Samsung Best Paper
- LG Best Paper
- IEEE CAS Seoul Chapter Best Paper
- IEEE EDS Korea Chapter Best Paper
- IEEE SSCS Seoul Chapter Best Paper
- COSAR Best Paper

**Poster Session**
- Samsung Best Paper
- IEEE CAS Seoul Chapter Best Paper
- IEEE EDS Korea Chapter Best Paper
- IEEE SSCS Seoul Chapter Best Paper

**Chip Design Contest Award**
- Best Design Award
- Altera Award

**Gift Drawing**

Participation awards are given in the end of closing ceremony.

**Reviewers**

Jin-Ho Ahn
Jin-hong Ahn
Sanghyeon Baeg
Sanghyeon Baeg
Hoon Chang
Beom Ik Cheon
Kyeongsoon Cho
Kyoungrok Cho
Byong-Deok Choi
Joo Sun Choi
Jun Rim Choi
Jung Yun Choi
Lynn Choi
Seung Jong Choi
Woo-Young Choi
Yungho Choi
Kukjin Chun
Eui-Young Chung
Ki-Seok Chung
Sung Woo Chung
Yungseon Eo
Gi-young Yang
Young-Mo Gu
Kilsik Ha
Gunhee Han
Tae Hee Han
Songcheol Hong
Ilsoon Jang
Youngbeom Jang
Deog-Kyoon Jeong
Gibong Jeong
Woojin Jin
Bongsoo Kang
Jin-Ku Kang
Sehyeon Kang
Sungho Kang
Yong-Seok Kang
Boeun Kim
Chang-Wan Kim
Daejeong Kim
Hi Seok Kim
Jae-Joon Kim
Jongmin Kim
Lee-Sup Kim
SeokYoon Kim
Shiho Kim
Sungchan Kim
Yongju Kim
Yong-Kweon Kim
Youjin Kim
Young Hwan Kim
Young-Kwang Kim
Bai-Sun Kong
Jaeyoung Kwak
Sunghoon Kwon
Chanzho Lee
Je-Hoon Lee
Jri Lee
Moon-Que Lee
Sang-Jeong Lee
Seongsoo Lee
Seung-Hoon Lee
Seungjun Lee
Seung-Sik Lee
Seung-Woo Lee
Yongsurk Lee
Young Keun Lee
Chun-Gi Lyuh
Byeong Min
Kyeong Sik Min
Yong Moon
Young Sun Na
Jinsoo Noh
Byeongha Park
Hong June Park
In-Cheol Park
Joonseok Park
Seong Hee Park
Sung Min Park
Jeongjin Roh
Jong-Kug Seon
Hyunchol Shin
Youngsoo Shin
Jae-Yoon Sim
Minkyu Song
Young-Jun Song
MyungHoon Sunwoo
Hyosig Won
Sung-Hyun Yang
Youngjoo Yee
Sungjoo Yoo
Kwang Yoon
Sungroh Yoon
Jaeeh You
Chong Gun Yu
Hyun-Kyu Yu
Conference Venue Map
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National Center for Nanomaterials Technology

Research Center
- International Atomic
- Electron Microscopy Center
- Center for SPM Standardization Research
- Center for Nano-Energy System Research

Synopsis
Name of project: National Center for Nanomaterials Technology
Period of project: August 1, 2004 - July 31, 2009
Host: POSTECH (Pohang University of Science and Technology)
Budget: USD 110 Million (Government: USD 40 Million + Concession 70 Million)
POSTECH Consortium: 130 Members

Mission
Establishment of NCNT equipped with core research facilities focused on nano-materials development
- Develop core technologies related to nanomaterials
- Create new industries related to nanomaterials
- Support the start-up and spin-off of new ventures
- Lead the next-generation growth-oriented industries

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THE CHIP INSIDE

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Information

Samsung Techwin has future-oriented goals. Samsung Techwin aims to be a leader that gives ultimate satisfaction to its customers in the era of digital technology.

<table>
<thead>
<tr>
<th>Number of Employees</th>
<th>5082 persons (December 31, 2007)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Sales in 2007</td>
<td>3,243 billion won</td>
</tr>
<tr>
<td>Address of the Head Office</td>
<td>Korea Invention Promotion Association 15th Floor, Yeokjang-dong 647-9, Gangnam-gu, Seoul, Korea</td>
</tr>
<tr>
<td>Representative Phone Number</td>
<td>82-2-3467-7114, 7000</td>
</tr>
<tr>
<td>Representative Fax Number</td>
<td>82-2-3467-7080</td>
</tr>
<tr>
<td>Major Products</td>
<td>Semiconductor Business Chip manufacturers, wire bonding, lead frame Optical &amp; Digital Imaging Cameras, CCTV, SVP, optical instruments Engine Business Aircraft engines, overhaul, turbo-machinery Defense Program 155mm SPH, KO Thunder, MSACE etc.</td>
</tr>
</tbody>
</table>

Vision

Technologies Designed to Enrich Digital Lifestyles

Digital technologies are revolutionizing our world and the way we live. Time and space are no longer the barriers to our aspirations they once were, and innovations turned things that were not long ago in the realm of science fiction into realities.

Life is more convenient and richer today thanks to digital technologies. Samsung Techwin, at the leading edge of the digital revolution, is continuously introducing life-enhancing innovations to the market in all of its business lines: namely, digital imaging, surveillance robots and energy.

Our Business

Optics & Digital Imaging...optical science and image processing technologies

Total Solution Provider...World class SMT, Semiconductor Assembly System

Everyday, Everywhere, for Everyone...Samsung Techwin, invisible power to open the digital world.

World’s First Technologies...There are technologies that move the world.

Defense Program...Technologies help maintain true peace

Quicker and Safer...We will save your precious time.

Chungbuk SoC R&D Center
Semiconductor Innovation Leader

Goal

Becoming a Leading Center of Semiconductor Industry through Strengthening SoC Design Ability

Business Supporting

- EDA Tools/Training
- Education of Design Methodology

R&D Linking

- Secure & Develop
- Dig up & Perform academic-industrial cooperative projects

Networking

- Organize & Operate “SoC Design Technology Exchange Council”
- Organize & Operate “SoC Cluster”

Supporting Programs

- Support joint R&D for SoC/embedded system
- Support EDA design tools & equipments
- Regular/customized professional technical education
- Provide IC manufacture one-stop service from design to test
- Support IP search/verification/modification/development
- Linking & Solving R&D troubles.

CHUNGBUK SoC R&D CENTER

Incubating & Bringing up

Chungbuk Technopark

Feel free to contact us at following address:
Tel: 82-43-241-1300 / E-mail: jameleda@cbtp.or.kr
www.cbtp.or.kr/ricbesoc
Questa® Functional Verification Platform
Integrated, standards-based platform delivering verification predictability and productivity

- Questa® multi-view verification components
- inFact™ intelligent testbench automation
- OVM proven, portable, reusable verification methodology
- Integrated assertions for fast debug and quality
- SystemVerilog mixed language leader
- High performance, high capacity simulation
- Efficient tracking of coverage to plan

Ask NeXilion!

Device name | feature
---|---
N5C302 | T-DMB Baseband-A/V decoder IC
N5C950 | T-DMB RF/Backband IC
N5C510 | DAB IC
N5C322 | ISDB-T one-seg A/V decoder IC

www.nexilion.com
Education project for promoting the use of semiconductor design property

Core-A

As part of the education project for promoting the use of Korean embedded processor Core-A, we would like to open undergraduate courses and nurture specialized lecturers to expand the Korean embedded processor market in an effective and efficient manner.

- Agreements for opening undergraduate courses
- Recruitment of lecturers specialised in embedded processor

Application deadline: December 6, 2008
Application method: Visit http://www.core-a.net/ and make an application at the menu "College Application"

KIPO
IDEC

유비쿼터스 환경하에서 시스템 설계 전문가를 위한 최상의 솔루션 라이브러리가 함께 합니다.

DSP Plus 5000
MATLAB & Simulink을 이용한 DSP 설계 솔루션

- DSP-Plus 5000은 기술적인 DSP 설계를 담당하는 소프트웨어로 평행으로 작동하는 DSP 프로그램을 구성하고 설계하는 데 사용됩니다. MATLAB과 Simulink을 이용하여 설계하는 데 도움이 됩니다.

- [실습 1, 2, 3]
  - MATLAB/Simulink 활용과 DSP 시스템 설계
  - MATLAB/Simulink 활용과 DSP 시스템 설계
  - MATLAB/Simulink 활용과 DSP 시스템 설계

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SYs-Lab 5000
Embedded System 정비

- SYs-Lab 5000은 FPGA 설계 및 배포를 위한绫 проведения 시스템 정비로 설계된 엑스케이브러시, Precedia의 마이크로소프트 Visio 프로토콜을 포함한 시스템 설계에 사용할 수 있는 일련의 시스템 정비 정비입니다.

- [ 실험 1, 2, 3, 4, 5 ]
  - 실험 1: 시스템 설계 및 설계
  - 실험 2: 시스템 설계 및 설계
  - 실험 3: 시스템 설계 및 설계
  - 실험 4: 시스템 설계 및 설계

[ 실험 1, 2, 3, 4, 5 ]
  - FPGA 디자인에 필요한 설정
  - 시스템 설계 및 설계
  - 시스템 설계 및 설계
  - 시스템 설계 및 설계

Korea Foundation for the Advancement of Science & Creativity

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